UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,176	06/30/2003	Steven H. Voldman	BUR920030009US1	1175

21918 7590 11/17/2005

DOWNS RACHLIN MARTIN PLLC
199 MAIN STREET
P O BOX 190
BURLINGTON, VT- 05402-0190

EXAMINER	
KITOV, ZEEV	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,176	VOLDMAN, STEVEN H.	
	Examiner	Art Unit	
	Zeev Kitov	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Examiner acknowledges a submission of the RCE request, Amendment and Arguments filed on August 5, 2005. Claims 3 – 5 and 9 are amended. Applicant's Arguments have been given careful consideration but they have been found non-persuasive. An Office Action follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. (US 6,624,660) in view of Lin et al. (US 6,473,282), and Texas Instrument Application Report SLYA014A. Li et al. disclose following elements of Claim 1 including an integrated circuit having: a substrate (P-SUB in Fig. 2B), a power rail (Vcc in Fig. 3) and a latchup control isolation network electrically coupled to the substrate, the latchup control isolation network adapted to electrically isolate the circuit from the power rail (col. 6, lines 36 – 67). It further discloses an active clamp network (elements 58, 64 and 52 in Fig. 3). However, it does not disclose in a case of a latchup isolating a sea of gates. Lin et al. disclose a sea of gates (elements 1 and 2 in Fig. 1, 8, 9, 10) being isolated by the latchup control isolation network (elements 3, 31 and 32 in Fig. 3). Both

references have the same problem solving area, namely providing the latchup isolation for CMOS integrated circuits. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Li et al. solution by adding the sea of gates according to Lin et al., in modern electronics the circuit block include plurality of gates; so the latchup protection circuit should be protected against latchup and as Texas Instrument Application Report states (on page 5, 4th paragraph), "the thyristor can be switched off again only by switching off the power supply", disconnection of the circuit from the power supply is the reliable way to end the latchup process. As to the claim limitation: "isolating sea of gates from said power supply in response to latchup event on said substrate", Texas Instrument Application Report shows (see Fig. 1 and 2, text on pages 3 and 4) that any latchup event involves flowing of substantial currents in the substrate through parasitic transistors. Therefore, involvement of substrate in the latchup events is inherent in the latchup effect.

Regarding Claim 6, Li et al. disclose the latchup control isolation network including the inverter circuit (element 64 in Fig. 3 playing the role of inverter with regard to element 52).

Claims 2 - 5, 7 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al. in view of Lin et al., TI Application Report and Blossfeld et al. (US 5,530,394). Claims 7 and 12 differ from Claim 1 rejected accordingly by their limitations of an active switching off network. Blossfeld et al. disclose the active switching off network (elements T14, T7, T9, T11, nD in Fig. 8, col. 6, line 39 – col. 7, line 37)

connected to the substrate (see Fig. 5). It further discloses turning off the latchup control isolation network, when connected in the prior step, thereby isolating the power rail from the protected circuit (col. 6, line 39 – col. 7, line 37). Both references have the same problem solving area, namely providing the latchup protection to the circuit (see col. 7, line64 – col. 8, line 2 in Blossfeld et al.). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Li et al. solution by adding the switching off circuit of Blossfeld et al., because as Blossfeld et al. state (col. 1, lines 11 – 31, col. 7, line 64 – col. 8, line 2), such solution provides the latchup protection to the system having multiple voltage supply sources.

Regarding claims 2 and 13, Blossfeld et al. disclose the substrate having a first polarity (substrate p- in Fig. 5), the circuit including a well having a second polarity (n- and n+ wells in Fig. 5). Even though the Fig. 5 does not show a whole latchup protection circuit, by a way of analogy, it is implicitly suggested that the circuit of Fig. 8 is designed the same way, i.e. the latchup control isolation circuit is also electronically coupled to the wells shown in Fig. 5 and is adapted to electrically isolate the circuit from the power rail in response to latchup events on the substrate (col. 7, line 64 – col. 8, line 2, col. 6, line 39 – col. 7, line 25). Lin et al. disclose the sea of gates and Blossfeld et al. disclose isolating by the switch off circuit (see rejection of Claim 1 above). The motivations for modification of the primary references are the same as above.

Regarding Claims 3, 14 and 17, Li et al. disclose the latchup control isolation network being turned off thereby isolating the protected circuit block from the power rail

when the voltage potential equals or is greater than a first predetermined value (col. 6, lines 36 – 67). It further discloses the substrate (shown in Fig. 2B), which inherently has a potential (col. 6, lines 27 – 35).

Regarding Claims 4 and 5, Li et al. disclose an integrated circuit including a well (28 in Fig. 2B), the power rail as being Vcc power rail (Vdd), and inherently posses a Vss power rail (shown as ground in Fig. 2B), and latchup control isolation network including a first FET with a first polarity type (52, 64 in Fig. 3) connected to the Vcc rail and a second FET (54, 62 in Fig. 3) with a second polarity type channel connected to the ground (Vss).

Regarding claim 8, Blossfeld et al. disclose the substrate having a first polarity (substrate p- in Fig. 5), the circuit including a well having a second polarity (n- and n+ wells in Fig. 5). Even though the Fig. 5 does not show a whole latchup protection circuit, by a way of analogy, it is implicitly suggested that the circuit of Fig. 8 is designed the same way, i.e. the latchup control isolation circuit is also electronically coupled to the wells shown in Fig. 5 and is adapted to electrically isolate the circuit from the power rail in response to latchup events on the substrate (col. 7, line 64 – col. 8, line 2, col. 6, line 39 – col. 7, line 25). Lin et al. disclose the sea of gates and Blossfeld et al. disclose isolating by the switch off circuit (see rejection of Claim 1 above). The motivations for modification of the primary references are the same as above.

Regarding Claim 9, Li et al. disclose the latchup control isolation network being turned off thereby isolating the protected circuit block from the power rail when the voltage potential equals or is greater than a first predetermined value (col. 6, lines 36 –

67). It further discloses the substrate (shown in Fig. 2B), which inherently has a potential (col. 6, lines 27 – 35).

Regarding Claims 10, 15 and 18, Li et al. disclose the first predetermined value as being close to Vdd or Vdd + Vbe (col. 6, lines 5 – 15).

Regarding Claim 11, 16 and 19, the explanation given by Li et al. (col. 6, lines 5 – 15) regarding the NMOS transistor (element 14 in Fig. 2A and B) cab be extended to the PMOS transistor (element 12 in Fig. 2A and B) with changing Vdd + Vbe to Vss – Vbe due to well known in the art mirror identity of NMOS/PMOS, NPN/PNP schematics. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Li et al. solution by adding the second predetermined value of Vss – Vbe for protection against latchup developing from the PNP parasitic transistor, because as well known in the art, due to the mirror identity of NMOS/PMOS, NPN/PNP schematics the same considerations of the latch up process initiation are valid for PNP parasitic transistor with Vss voltage playing the same role as Vdd for NPN transistor.

Response to Arguments

Applicant in his Arguments attacks the references of Li et al., Lin et al. and Myamoto alleging that due to their differences the references cannot be combined together.

1) Applicant alleges: "Li et al. teaches a mixed voltage floating well driver. All mixed voltage interfaces driver networks are inherently latchup immune in a CMOS

output driver. As such ..... the LI et al. reference is not believed to be relevant to the field of technology at issue in claim 1". However, according to Wai-Ming et al. (US 5,543,650), in the mixed voltage interfacing applications (col. 1, lines 46 – 60), the latchup immunity is a concern for mixed voltage interfaces, which is to be addressed (col. 5, lines 36 – 44).

2) In a second paragraph (page 8), the Applicant continues his attack on references saying: "it is inappropriate to combine the mixed voltage interface output driver of Li et al. with a "sea of gates". The sea of gates" is not a mixed voltage interface output driver design environment". However, the Pequignot et al. (US 6,157,530), the patent having the Applicant as one of the inventors, discloses the mixed voltage interface circuitry used in the "sea of gates" environment (col. 1, lines 19 – 25, Fig. 3, 4, col. 10, lines 30 – 50).

Therefore, the recited Applicant's Arguments regarding the two references are baseless.

Arguments regarding the Miyamoto reference are moot, since the reference is not used in the Office Action.

As to Applicant's criticisms of the Blossfield reference, it attacks the Blossfield alleging that the Blossfield circuit does not isolate the circuit form the power supply rails thus not providing claimed protection. However, Bloosfiled explicitly states (col. 7, line 64 – col. 8, line 15) that his circuit disconnects the first current bank m1 from the power supply. It further alleges that Blossfield does not address the latch up problem. However, Blossfield explicitly states (col. 7, line 64 – col. 8, line 15) that in his circuit "a

safe operating mode is reached in which the overall circuit can no longer latch up in an undefined mode when if the supply voltage Vdd is still relatively low". Therefore, Blossfield does addresses the latchup problem.

Applicant further attacks the Bollsfield on a ground that it does not disclose the "sea of gates". In response to such piecemeal analysis of the references, it has been held that one cannot show non-obviousness by attacking references individually where, as here, the rejection is based on combination of references. *In re Keller, 208 USPQ* 871 (CCPA 1981).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K. 11/14/2005

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800